An Implementation of a Real-Time and Parallel Processing ECG Features Extraction Algorithm in a Field Programmable Gate Array (FPGA)

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Abstract

The objective of the paper is to report a development of real-time and parallel processing algorithm to implement it into a Field Programmable Gate Array (FPGA) for the electrocardiogram (ECG) signals feature extraction. The prototyped system will be extracting the ECG features and tested as a System on Chip (Soc) design. The performance of algorithm was tested against MATLAB routine and validated results based on the MIT-BIH Arrhythmia database which has been annotated by cardiologists. The ECG signals from five volunteers were acquired, tested, analyzed and displayed in on line. This overall detection tolerance of the algorithm was 0.01 seconds.

1. Introduction

Many sophisticated algorithms have been proposed to improve the accuracy of prediction for electrocardiogram (ECG) waveform classification. There were methods of the principal component analysis (PCA), the adaptive resonance theory (ART), the wavelet neural network (WNN), or the fuzzy neural networks (FNN) [1]. The successful and important to reach their goal is to have an accurate extraction of ECG features. Therefore, among these methods, many have created hybrid classification systems to increase the accuracy of ECG features prediction [2-4]. However, these method and algorithms were performing better using post and offline processes to extract or to predict the feature and parameters of ECG.

For a homecare ECG monitoring device, it is important to extract the features of the ECG signal in real-time. The ECG feature such as R-R interval, QRS amplitude and duration, the magnitude and duration of p wave, potential of S-T segment [5], and the magnitude and duration of T wave are important for homecare applications. For example, the information or feature of R-R interval can be derivate to analyze the heart rate variability (HRV). The duration of QT interval can be used to determine the status of myocardial repolarization.

The objective of this abstract is to report a successfully development of a real-time ECG features extraction algorithm that could be implemented using Field programmable Gate Array (FPGA) device using parallel processing hardware. The implemented System on Chip (SOC) using FPGA that could be used to acquire digital ECG data from an Analog-to-Digital Converter (ADC), to display ECG and extracted information on a VGA type LCD device, to store the acquired ECG and the extracted information into a flash memory chip and to communicate to a PC computer using an USB device. The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL). It will be analyzing the component of the ECG signals and extracted 12 features of ECG information in real time within two heart beats. The system will be using these features primarily to identify the abnormal rhythm of heart beat.

2. Method and material

The algorithm will be analyzing the component of the ECG signals and information in real time for identifying the abnormal rhythm and heart beat. The programmed System on Chip (SoC) will be controlling the detection and digitizing ECG, analyzing and extracting feature of ECG, monitoring the information update to the LCD, interfacing with USB and Flash Memory. In this way, both the ECG signal in real time and the analyzed information can be displayed on the LCD panel. The information can be transmitted and presented using self-developed software that is designed with Borland C++ Builder through USB device. The ECG data from MIT-BIH database could be input from hosted PC to the prototype system by USB bridge device.

The real-time ECG acquired and digitized data could be input to the prototype system directly. These data paths were shown in Figure 1. The acquired data, inputted data and result of the data processing could be shown at LCD display in real-time, stored in Flash memory or transmitted to host PC by user selection.

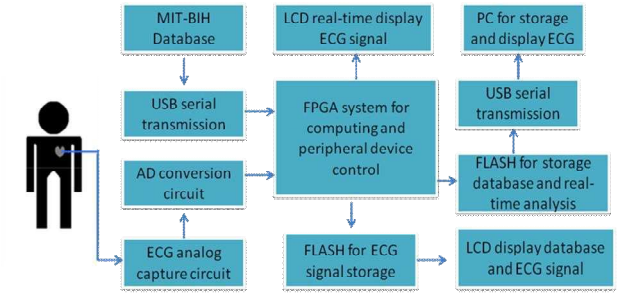

Figure 1. The processes of prototyped system was shown as system block diagram which includes a digital ECG data input, two Flash memories, control buttons, LCD Display and USB communication.

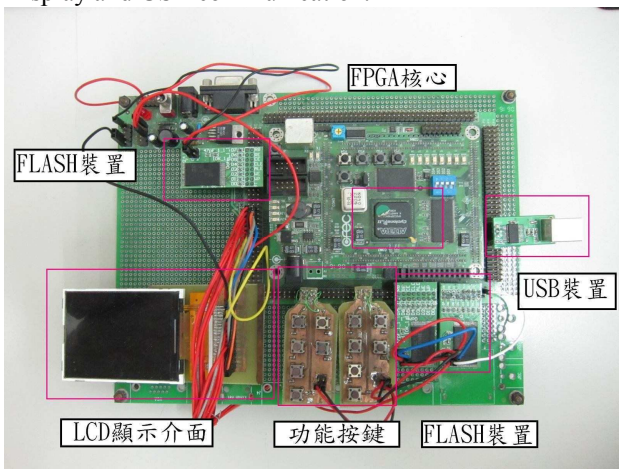

Figure 2. Prototype System block Diagram at the upper panel and the picture of integrated system at the lower panel with digital ECG data input, two Flash memorys, control button, LCD Display and USB communication.

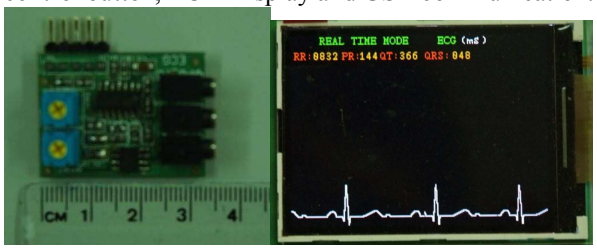

Figure 3. ECG amplifier at the left panel and the acquired ECG LCD display at the right panel.

For the real-time ECG feature extraction, a pipe-lined has been setup within the FPGA that governments and distributes data to individual feature detection module, e.g. peak detection, or zero crossing module. The pipe-lined buffer was using proper First-In-First-Out (FIFOs) buffer to control the data flow and timing sequence.

The ECG feature detection procedure has started from recognizing the R-peak. The registered R-peak will be setting off buffered data and look for P wave and Q wave. The same signal will be triggered modules to look for S wave and the start of T wave, and end of T wave from previous heart beat. In this way, the timings of features were recorded, stored and transmitted.

3. Result

The performance of algorithm developed and embedded in FPGA was tested and validated using the MIT-BIH Arrhythmia annotated database against the result from MATLAB. This overall average R-peak timing detection difference against the annotated data (250Hz) to the algorithm data was 0.25±0.45 sampling point and is 0.001±0.0018 seconds, shown in Table 1. The detection error for the MatLab procedure against MIT-BIH annotated data was 0.3±0.47 sampling point. For the timing of Q-peak detection difference, it was -2.05±1.76 sampling points for the embedded procedure in FPGA, and, the detection difference for the MatLab procedure -0.45±1.31 sampling points, as shown in Table 2. The timing of end of T wave detection difference was shown in Table 3. The detection error for MatLab procedure was 1.05±0.4 sampling points. And, the detection error for FPGA procedure was 0.52±0.69 sampling points.

Table 1. R peak detection for MIT-BIH Sample 231

MATLAB	MIT-BIH	FPGA	MatLab Detection	FPGA Detection
376	375	375	1	0
609	609	609	0	0
842	841	842	1	1
1072	1072	1072	0	0
1299	1299	1299	0	0
1550	1550	1550	0	0
1794	1794	1794	0	0
2032	2032	2032	0	0
2274	2274	2274	0	0
2517	2517	2517	0	0
2749	2749	2749	0	0
2992	2992	2992	0	0
3230	3229	3230	1	1
3459	3459	3459	0	0
3685	3684	3685	1	1
3920	3919	3920	1	1
4145	4145	4145	0	0
4377	4376	4377	1	1
4611	4611	4611	0	0
4835	4835	4835	0	0
Mean Error in Sampling Points			0.3	0.25
Standard Error in Sampling Points			±0.47	±0.45

Table 2. Q wave detection for MIT-BIH Sample 231

MATLAB	MIT-BIH	FPGA	MatLab Detection	FPGA Detection
364	364	364	0	0
599	599	598	0	-1
832	832	830	0	-2
1062	1065	1060	-3	-5
1289	1289	1287	0	-2
1540	1540	1538	0	-2
1784	1788	1782	-4	-6
2022	2022	2019	0	-3
2263	2264	2262	-1	-2
2507	2510	2504	-3	-6
2738	2738	2736	0	-2
2982	2982	2980	0	-2
3219	3219	3218	0	-1
3449	3449	3447	0	-2
3674	3674	3674	0	0
3910	3910	3909	0	-1
4135	4134	4134	1	0
4367	4366	4365	1	-1
4600	4600	4599	0	-1
4825	4825	4823	0	-2
Mean Error in Sampling Points			-0.45	-2.05
Standard Error in Sampling Points			±1.31	±1.74

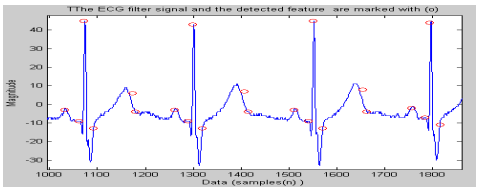

Figure 4. The extracted features of ECG were marked onto a MIT-BIH Sample 231 ECG data.

The prototype system has been tested in real-time. The system has been tested to acquire ECG signals and the features of ECG has been extracted from five volunteers in real-time and on line. And, the data and the analyzed results were shown in Figure 5. For the continuous 10 minutes real-time ECG tests, one of the result was shown at Figure 6. The figure was showing the average sampling points difference for the interval of RR, PR, QT and QRS duration. For RR interval, the difference was 2 sampling points and the standard error was 1 sampling points.

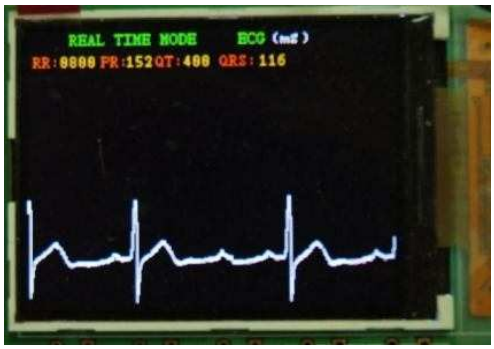

Figure 5. The panel was displaying a real-time ECG of a volunteer.

Table 3. T wave detection for MIT-BIH Sample 231

MATLAB	MIT-BIH	FPGA	MatLab Detection	FPGA Detection
464	463	463	1	0
693	692	693	1	1
928	927	928	1	1
1157	1156	1156	1	0
1388	1387	1387	1	0
1637	1636	1636	1	0
1884	1883	1883	1	0
2118	2118	2117	0	-1
2360	2359	2359	1	0
2603	2602	2602	1	0
2837	2836	2837	1	1
3076	3074	3075	2	1
3322	3321	3322	1	1
3547	3546	3546	1	0
3770	3769	3770	1	1
4011	4009	4011	2	2
4232	4231	4232	1	1
4461	4460	4461	1	1
4702	4701	4702	1	1
Mean Error in Sampling Points			1.05	0.52
Standard Error in Sampling Points			±0.40	±0.69

4. Conclusion

The objective is to develop an algorithm for processing the electrocardiogram (ECG) signals that will be extracting the ECG features and to implement it using

the FPGA as a testing prototype for System on Chip (Soc) design. The algorithm will be analyzing the component of the ECG signals and information in real time and to identify the abnormal rhythm and heart beat. The program controls the detection, analysis and monitoring of the LCD, USB and Flash Memory of the FPGA. Both the ECG signal in real time and the analyzed information can be displayed on the LCD panel. The information can be transmitted and presented using self-developed software that is designed with Borland C++ Builder through USB device.

The performance of algorithm was tested using MATLAB and validated based on the MIT-BIH Arrhythmia database which has been annotated by cardiologists. This overall detection tolerance of the algorithm was 0.02 seconds. The prototype system has been tested in real-time. The ECG signals from five volunteers were acquired, tested and analyzed and displayed in on line.

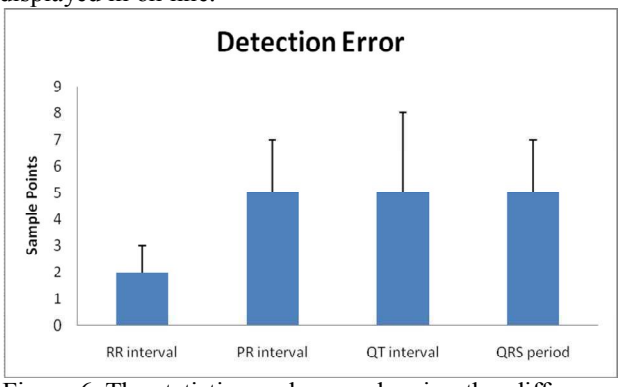

Figure 6. The statistic graph were showing the difference of the extracted features for the 10 minutes of data.

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